ABSTRACT

A semiconductor protection element is provided in which no heat generation occurs in a concentrated manner, in a region having a high resistance value even when electrostatic discharge (ESD) is applied, without an increase in an area of the semiconductor device. The semiconductor protection element is made up of an N-type well, P-type semiconductor substrate having a pair of N^+ diffusion layers each having an impurity concentration being higher than that of the N-type well, and a silicide layer partially formed on each of the two N^+ diffusion layers. The N-type well has a first exposed region being exposed on the semiconductor substrate and the silicide layer is so formed that a part of each of the two N^+ diffusion layers has a second exposed region being exposed successively so as to be in contact with the first exposed region. The first exposed region is sandwiched by two N^+ diffusion layers.